Evolvable Hardware or Learning Hardware?
Induction of State Machines from Temporal Logic Constraints

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Abstract

Here we advocate an approach to learning hardware based on induction of finite state machines from temporal logic constraints. The method involves training on examples, constraints solving, determinization, state machine minimization, structural mapping, functional decomposition of multi-valued logic functions and relations, and finally, FPGA mapping. In our approach, learning takes place on the level of constraint acquisition and functional decomposition rather than on the lower level of programming binary switches. Our learning strategy is based on the principle of Occam's Razor, facilitating generalization and discovery. We implemented several learning algorithms using DEC-PERLE-1 FPGA board.

1 Evolving in hardware versus learning in hardware

In recent years the scientific community has witnessed rapid developments in the area of Soft Computing. These approaches include Artificial Neural Nets (ANNs), Cellular Neural Nets (CNNs), Fuzzy Logic, Rough Sets, Genetic Algorithms (GAs), Genetic and Evolutionary Programming.

Several mixed approaches have also been created. In different ways, they combine elements of these areas with the goal of solving complex and poorly defined problems that could not be tackled by earlier, analytic models. What is common to all these approaches is that they propose a way of *automatic* learning by the system. The computer is taught by examples rather than completely programmed (instructed) in what to do. This philosophy also dominates areas of Artificial Life, solving problems by analogy to nature, decision making, knowledge acquisition, and new approaches to intelligent robotics. Machine Learning thus becomes a new and general system design paradigm unifying these previously disconnected research areas. It starts to become a new hardware construction paradigm as well.

Recently, the term Evolvable Hardware (EHW) has been coined [15] which means the realization of genetic algorithm (GA) in reconfigurable hardware. It is exemplified by Brain Builder CBM [15]. The EHW approach to computing has raised considerable interest and enthusiasm among some researchers, but scepticism among others. One may ask: "Why *genetic* algorithm"? Our experience prompts us to question the usefulness of GA as a sole learning method to reconfigure binary FPGAs. Instead, we propose the Learning Hardware approach, which consists in using feedback from the environment (for instance, positive and negative examples from the trainer) to create a sequential network and subsequently realizing this network in FPGAs.

Our approach of Universal Logic Machine [35, 40, 38, 24, 37, 45] proposes the creation of a learning machine based on logic principles, in particular, temporal logic [32, 4, 5, 6, 7], constructive induction [2, 11, 27, 28], and rough set theory [34].

Our software algorithms require fast operations on complex logic expressions and the ability to solve NP-complete problems such as satisfiability. They should be realized in hardware to obtain the necessary speed-ups. Using a fast prototyping tool, the DEC-PERLE-1 board based on an array of Xilinx FPGAs, we are developing software/configware processors that accelerate the acquisition, synthesis, and optimization of Reactive State Machines.

While GA is a simple and practically blind mechanism of Nature, it can be easily realizable in hardware. We believe that this mechanism alone cannot produce good results.

(Although it is relatively easy to do crossover and mutation in hardware, the fitness function evaluation is difficult). In contrast, logic algorithms that draw upon human knowledge are optimal and mathematically sophisticated. They lead to high quality learning results: knowledge generalization, discovery, no overfitting, small learning errors [47, 1, 26, 20, 21]. Their software realizations, however, use such complex data structures and controls that it is difficult to realize them in hardware.

When we refer to **Learning Hardware**, we define the term "learning" very broadly, as any mechanism that leads to the improvement of operation; evolution-based learning is therefore included. Although specific learning concepts and their formalities differ from one learning approach to another, what is common is that, in the process of learning, a network (combinational or sequential) is constructed that stores the knowledge acquired in the learning phase. The learned network is next run on old or new data. Responses may be correct or erroneous. The network's behavior is then evaluated by some fitness (cost) functions and the learning and running phases are alternated.

The process of solving problems consists of two phases: **the phase of learning**, which involves constructing and tuning the network, and **the phase of acting**. The second stage means using knowledge, that is, running the network for data sets. Compared to the process of developing and using a computer, the first stage can be likened to the entire process of conceptualizing, designing, and optimizing a computer, and the second stage to using this computer to perform calculations. You cannot redesign standard computer hardware, however, when it cannot solve a problem correctly. The Learning Hardware will redesign itself automatically using the new learning examples provided to it.

2 Logic rather than evolutionary methods for learning

Our ULM approach is based on FPGA technology and associated logic development methods (called Logic Synthesis by the design automation community and Constructive Induction by the Machine Learning community) rather than neural or genetic algorithms. Michie [29] makes a distinction between black-box and knowledge-oriented concept learning systems by introducing concepts of weak and strong criteria. The system satisfies a weak criterium if it uses sample data to generate an updated basis for improved performance on subsequent data. A strong criterion is satisfied if the system communicates concepts learned in symbolic form [28].

Let us observe that ANNs, CNNs, and similar approaches satisfy only the weak criterium while our approach satisfies the strong criterium. We believe that the results of the learning process, and even the process itself, should be rational. They should be similar to those of teaching humans, based on symbolic logic and not on the methods of Nature. Human thinking consists in abstract use of symbols, rather than assigning numeric weights to neurons. Our approach operates on higher and more natural symbolic representation levels. The built-in mathematical optimization techniques (such as graph coloring or satisfiability) support the principle of Occam's Razor, offering solutions that are provably good in the sense of Computational Learning Theory (COLT) [1. 47]. **Thus, learning on a symbolic level is the first main point of our approach.**

In our past research, we have used and compared in software, various network structures for learning: two-level AND/OR (Sum-of-Products (SOP), or Disjunctive-Normal-Forms (DNF)) [33], decision trees (C4.5), and multi-level decomposition structures [20, 21, 36, 53, 44], as well as various logic, non-logic and mixed optimization methods: search [37], rule-based, set-covering, graph-coloring, genetic algorithm [16, 18] (including mixtures of logic and GA approaches), genetic programming [17], artificial neural nets, and simulated annealing. We compared the resulting complexity of our networks (Occam's Razor), as well as various ways of controlling the number of errors in the learning process [20, 21, 26]. The Decomposed Function Cardinality (DFC) and its extensions for MV logic [1, 20, 21, 44] were used as common measures of complexity, because of their strong theoretically proven properties [1, 47]. Our conclusion, based on these investigations, is that logic approaches and especially the MV decomposition techniques, combined with smart heuristic strategies and good data representations, are usually superior to other approaches due to smaller net complexity and fewer learning errors.

In our experience, especially poor results are obtained using genetic algorithms [16, 17, 18]. GA may perform well in other applications, but from both our experience and the literature we could not find a single problem domain in which a GA-based algorithm was superior to a hand-crafted algorithm in the design of a binary or multi-valued logic network. This is perhaps because researchers have long experience in creating efficient logic minimization algorithms (for instance, more papers have been written on SOP minimization than perhaps on any other engineering topic). In our approach we want to make use of this accumulated human experience, rather than to "reinvent" algorithms using GA.

3 Learning hardware approach in universal logic machines

Developers of evolvable and learning systems agree that, realized with current software or even parallel programming technologies, the learning phase and/or the execution phase are too slow for real-life problems, especially real-time problems. The situation is essentially the same regardless of whether the exhaustive combinatorial search, simulated annealing, or evolutionary algorithms that involve millions of populations are used. Thus, the researchers proposed to speed-up some phases by migrating from software to hardware.

Many ambitious projects based on ANNs, cellular logic, DNA, simulated evolution and biologically motivated hardware have been proposed that will perhaps be successful in the future, when realized on molecular or quantum levels. However, many of them are quite impractical in current technologies.

Most of the approaches to evolvable hardware use binary Field Programmable Gate Arrays, because now there is simply no other mass-scale hardware reconfigurable (reprogrammable) and relatively inexpensive technology widely available. Since in binary FPGAs everything is realized on the level of binary logic gates and flip-flops, in our opinion, the learning process should be performed on this level also. **Thus, learning on the level of logic gates and flip-flops is the second main point of our approach.**

We believe that the learning level of sequential logic nets is more natural than the higher level of arithmetic operations of ANNs or Fuzzy Logic functions, or the lower level of routing FPGA connection paths. Once we decide to realize the network using logic gates in FPGA, we should apply efficient logic design algorithms and **realize them in hardware for speedup**. We believe also that all methods that exist in VLSI design, and especially, the powerful EDA (Electronic Design Automation) tools, should be re-used in their entirety, rather than duplicated by naive low-level evolutionary algorithms. Engineers spent many years developing such tools in the area of digital design automation; especially for reconfigurable computers: state machines, logic synthesis, technology mapping, placement and routing, partitioning, timing analysis, etc. Their use will facilitate creation of Learning Hardware. Occam Razor principle should also be used because only it leads to meaningful discoveries and explainable results.

In conclusion, we do not believe that the "purist strategies" for evolutionary hardware are practically acceptable for most commercial applications of Learning Hardware. Therefore, we propose the concept of Learning Hardware based on previous human problem-solving experience and application of mathematical algorithms and problem-solving strategies rather than relying on two basic methods to Evolvable Hardware: ANNs and GA. Learning/evolution will remain as the main principle of building new generation hardware, but it should be restricted to higher, abstract levels rather than lowest level FPGA resources. The variant evaluation/selection should also be performed on abstract levels, before mapping to low-level field-programmable resources, for which chromosomes are extremely long and the GA is very inefficient.

The proposed ULM approach to Learning Hardware can be summarized as follows:

1. Based on sets of examples specified in our input language L, we create a Reactive State Machine (RSM), in particular, a (combinational) function or a relation with no temporal variables. The description consists in input-output specification, initial state specifications and global environment constraints. This machine is usually non-deterministic, but is state-minimal from construction [4, 5, 6, 7]. with respect to all its variables as state variables.
2. The machine can be determinized (converted from non-deterministic to deterministic form). Next the machine is state-minimized (with respect to the new set of state variables, which are a subset of initial input/output variables). We plan also to develop a method to get a state-minimal determinization right away.
3. The machine is mapped to constrained structural resources which we call Regular Automata (RA). It assumes some regular structure, such as a counter, shift register, cellular automaton, or any local-connection based sequential network, and checks for the maximum isomorphism between the autonomous state transition graph of this network and the RSM graph. (The new methods of mapping a state machine to a counter or a shift register are both part of our methodology).
4. The time-based MV logic expressions of Regular Automata are decomposed. We use the algorithm which is our generalization of the functional Ashenhurst-Curtis decomposition [36, 44]. The timed variables, and the multi-valued variables, are converted to new binary variables.
5. The (quasi)optimally constructed network is logically mapped to standard FPGA CLBs and realized using standard partitioning, placement, and routing with the help of EDA tools from Xilinx or other companies. Thus, each RSM is converted to a binary pattern of programming switches in FPGA.
6. The knowledge of the machine is stored in binary memory patterns representing final FPGA reconfigurable information. Under supervision of the software program, the hardware switches between a number of evolved circuits, depending on rules that

can also be acquired automatically. This phase is therefore similar to the CBM approach of DeGaris.

7. As the network solves new problems, the new data sets and training decisions are accumulated and the network is repeatedly redesigned. An old network can serve as a redesign plan for a new network, or the latter is "designed from scratch" to avoid any bias.

Thus, we replace the process of creating high level behaviors by evolving on low level used in EHW, with the ULM model of learning at high level and next compiling to low level using standard FPGA-based tools. Observe also that the same physical FPGA resources are multiplexed to implement the virtual human-designed **learning hardware** and the automatically learned **data hardware**. While the "learning hardware" is designed once and cannot be changed, the "data hardware" can be modified indefinitely.

4 Induction of reactive state machines from temporal logic constraints

Because decompositions of combinational logic have been already explained in detail in our previous papers [20, 21, 26, 32], here we concentrate on Reactive State Machines. As explained in the previous section, when the expression (set of examples) in the input language has been created, the problem is closed and becomes that of designing the minimal state machine using regular binary resources of lookup-tables and flip-flops. Our state machine design integrates methods developed in USA and former USSR. We introduce new efficient and practical methods for specification and synthesis of state machines [4, 5, 6, 7, 32] that can significantly improve the solutions currently used in the United States. Developed in the major computer centers of the former Soviet Union, these methods were never published in English or presented to American audience.

Theoretically, any FSM-based EDA tools can be used to solve these tasks. There are, however, some specifics of our approach, which make it different in practice. These differences are related to two issues: (1) The use of temporal logic as the input specification. (2) The use of Regular Automata for structural design.

4.1 Temporal logic

While the temporal logic has been used in the West for verification, there are no papers on its applications in synthesis. At the same time, this logic was used in former USSR for synthesis as well [4, 5, 6, 7, 32]. In addition, to make it compatible with our decomposer, we extend this logic to multi-valued logic data.

In contrast to logic circuit design, the learning data are extremely weakly specified, it is common to have a function or a machine with 99,999% of don't cares. Current EDA software cannot handle such data well, if at all. This fact affects all synthesis algorithms.

Also, we are not familiar with tools that would create a non-deterministic FSM first, and next convert it to a deterministic one. So far, such tools were used only for verification(reachability analysis). Also, state minimization is now an important part of synthesis of strongly unspecified FSMs.

4.2 Regular automata

To convert a deterministic or non-deterministic machine to sequential network from CLBs (lookup tables and flip-flops), instead of a standard state assignment/ minimization-factorization/ FPGA mapping process, we use the structural synthesis mapping approach based on Regular Automata (RA) design and functional decomposition. Because it is oriented towards lookup-tables, mapping from our RA intermediate format to real chip resources is relatively easy. Good decomposition leads to feature extraction (discovery) and generalization.

This approach is well suited to geometrical constraints imposed on sequential logic, thus it is called the Regular Automata approach. Regular Automata include Cellular Automata as their special case, but every automaton in the array can be different, the connections can be to many nodes, not only to closest geometrical neighbours, etc. More specifically, by Regular Automata we understand sequential netlists placed on a two-dimensional grid in such a way that most of the connections are local, it means, they are to cell's neighbors only, plus there are some global buses and collectors. Every cell may include a number of flip-flops and programmable gates and be connected to two, three, four, eight, twelve, etc neighbors and buses. For instance, there are four neighbors, two vertical and two horizontal buses in the Concurrent Logic Inc. (now ATMEL) architecture [9], which is a special case of our previous model of Regular Layout [41, 42, 43, 49, 50]. Regular Layout is extended to Regular Automata by just adding flip-flops to cells. Flip-flops can be: standard (D, T, JK); and non-standard (half of JK, and START, or logic differentiation [10]). In addition to vertical and horizontal buses, we allow also for diagonal buses. Other examples of Regular Automata are Iterative circuits, Lattice Diagrams, Cellular Automata, counters, shifters, and similar circuits. Practical realizations of Regular Automata are also: the ILU of the CCM [40], and the satisfiability/ESOP minimization machine from [37].

Our methods can preserve partially the structure defined by the original specification and facilitate the design flow that is *transparent* for the designer (graphs of RSMs and autonomous machines are visualized - Fig. 1). The latter is

able to supervise the process and influence it when necessary, for example, by changing state encoding or ensuring the proper timing properties. In this way, the designer is not faced with the ready-made results of synthesis as in some of the modern high-level synthesis tools, which mostly rely on incremental synthesis, but is able to quickly produce the effective designs. An interesting aspect is ability to modify the constraints when the designer is not sure of his intention: he experiments with constraints and verifies his ideas on the graphs.

5 Input language to represent learning data

Because we want the system to learn on a higher level than that of elementary gates and their connections, we need first to develop a higher-level language, in which expressions, the virtual nets, will be automatically created, evaluated, selected and optimized, in order to be realized as hardware FPGA nets by top-down automatic design methods. Since in the learning phase we want to operate on elements of this language in hardware, our choices are limited because of the necessity of operations that are easily realizable in hardware.

Several such languages have been created in the past, mostly for applications in logic synthesis, automatic theorem-proving, data base theory, and Information Engineering, and we adopted some of them for hardware representation. They include: temporal logic, regular expressions, Petri nets, state machine tables, tabular representation of data [8], binary and multi-valued cube calculus [12, 40], decision tables, rough sets [34], rough partitions [25], and labeled rough partitions [22].

Table 1. Multi-valued multi-output (combinational) relation in tabular form

	x_1	x_2	y_1	y_2
a	0, 2	1	—	2
b	0, 1	0	0, 2	1
c	2	0	1, 2	0
d	1	1	1, 2	2

A universal language to specify MV combinational logic is a two-dimensional tabular representation, as shown in Table 1. Rows correspond to objects (examples, samples) *a*,*b*,*c* and *d* and columns to input variables (attributes) x_1 and x_2, and output variables y_1 and y_2. Symbol y_1 denotes a relation output. Inputs x_1 and x_2 together with output y_1 specify an (oriented) relation. Relation can be used to express such facts as: this color is *red* or *white* but not *yellow* or *black*. Symbol y_2 denotes a function output; y_2 $(x_1\ x_2)$. Rows *c* and *d* have only one value for each attribute, so they are *minterms*. Rows *a* and *b* have more than one value for attributes, so they are *cubes*. Eeach row can be thought of as a record from a data base, or their set, or a collection of image features after image preprocessing.

Observe, however, that although such language is quite powerful for machine learning, data mining and knowledge discovery from data bases applications, it cannot specify time, it is thus too poor to describe state machines, regular expressions, Petri nets, path expressions, sequential netlists, grammars and other models, that are used in speech and image recognition, robotics, and other areas. Extension of this language can be done by introducing variables that depend on discrete time. For instance, the example *a* (row *a*) from Table 1 can be rewritten to our language as follows:

$x_1[0,2](t)\ \&\ x_2[1](t) \Rightarrow y_2[2](t)$,

because both input variables $x_1(t)$, $x_2(t)$ and the output variable $y_2(t)$ are defined in the same moment of time. By allowing previous or next ticks of time, for instance:

$x_1[0,2](t\text{-}2)\ \&\ x_2[1](t\text{-}3) \Rightarrow y_2[2](t+3)$,

we can specify arbitrary regular grammars, regular expressions, sequential netlists, or state machines with multi-valued inputs and outputs. Timed binary variables are next internally converted to standard binary variables, for instance, `x(t)=>x, ~x(t-1)=>x', x(t-2)=>x"`, etc. Similarly, timed MV variables are internally converted to standard binary variables. Various binary encodings of MV symbols can be used.

To understand the power of our language, we successfully described problems, such as "cannibals and missionaries", "man, wolf, goat and cabbage", "dining philosophers", models of Pavlov's behaviors, various real-time protocols, and other problems specified by temporal logic constraints. We noticed for MV logic only two simple generalizations are needed: (1) adding time moments to logic variables and (2) allowing the formulation of equations not only in an explicit way (the output variables as the functions of the input variables) but also as non-explicit, convoluted MV equations involving input, output, and auxiliary (state, constraint) variables. These allow us to create a language of high expressive power which is also quite natural. The language allows specification of temporal and logic constraints, such as "the man cannot be lazy, he has to move the animal or the item to another shore of the river", "cannibals cannot row", or "only three people can be in the boat").

Let us consider one example of temporal logic specification used in our methodology. This is the well-known problem of the man, the wolf, the goat, and the cabbage. At the beginning, all of them are on the left bank

of the river, and the man should transport them to the right bank. The wolf and the goat, as well as the goat and the cabbage, cannot be left alone on the same bank without man. The boat is navigated by the man, who can take only one object with him.

All the boolean variables are first-order predicates depending on discrete time. *M(t)* is true when the man in the left bank and false when the man in on the right bank. The same applies to variables *W(t), G(t), C(t),* which denote the wolf, the goat, and the cabbage respectively.

Here is the temporal logic specification of constraints for this problem.

1 The wolf and the goat cannot stay on the left bank and on the right bank without the man:

```
(  W(t) &  G(t) ) => M(t).
( ~W(t) & ~G(t) ) => M(t).
```

The goat and the cabbage cannot stay on the left bank and on the right bank without the man:

```
(  G(t) &  C(t) ) => M(t).
( ~G(t) & ~C(t) ) => M(t).
```

2 If the wolf is on the left (right) bank, it means that either the wolf stayed there or the man has brought it there from the right (left) bank one unit of time before:

```
 W(t) =>( W(t-1) |~W(t-1)&~M(t-1)& M(t) ).
~W(t) =>(~W(t-1) | W(t-1)& M(t-1)&~M(t) ).
```

The same for the goat and the cabbage:

```
 G(t) =>( G(t-1) |~G(t-1)&~M(t-1)& M(t) ).
~G(t) =>(~G(t-1) | G(t-1)& M(t-1)&~M(t) ).
 C(t) =>( C(t-1) |~C(t-1)&~M(t-1)& M(t) ).
~C(t) =>(~C(t-1) | C(t-1)& M(t-1)&~M(t) ).
```

3 Any two objects cannot be brought across the river at the same time:

```
(W(t) <=> W(t-1)) | (G(t) <=> G(t-1)).
(W(t) <=> W(t-1)) | (C(t) <=> C(t-1)).
(G(t) <=> G(t-1)) | (C(t) <=> C(t-1)).
```

4 The man is always on the move:

```
M(t-1) <=> ~M(t).
```

Here the symbols ~, &, |, =>, and <=> designate complemented variable, logic AND, logic OR, logic implication (*~a& b*), and logic equivalence (*a&b |~a&~b*), respectively.

The result of synthesis from this specification using our software system DUAL is shown in Figure 1. The state transition graph given in dotted lines corresponds to the non-deterministic algorithm, which the man should follow to safely transport all the objects to the right bank. This algorithm consists of seven steps, with two possible variations, depending on whether he chooses to take the cabbage or the wolf when the goat is already trasported to the right bank. Observe that the designer (the supervisor, the environment), who gives the language L expressions to the learning system, does not know the state machine, he only specifies constraints on the behavior of the system or sample sequences of input and output values.

6 DEC-PERLE-1 board for fast prototyping

The DEC-PERLE-1 board [52] is organized around a central computational matrix made up of 16 Xilinx XC3090 LCAs[1], surrounded by four 1MB RAM banks, and 7 other LCAs to implement switching and controlling functions. We modeled our algorithms in software. We also realized the first version of ULM, called Cube Calculus Machine (CCM) on DEC-PERLE [24, 37, 38]. These were very useful learning experiences. The DEC-PERLE-1 board, similar to other FPGA boards, advocates **regular design styles** without many control signals. It is then good for small SIMD processors, pipelining, systolic processors, Cellular Automata or complex (decomposed) Boolean functions. The basic design principle is the following: **map two-dimensional tables to two-dimensional logic resource arrays**, leading to the introduction of the concept of Regular Automata. The design can be developed incrementally thanks to its easy memory access, host interface with FIFOs, and the clock debugging modes and tags. Based on these principles, we next developed a new variant of the Cube Calculus Machine and evaluated its speed-up. The goal is now to map software algorithms such as binate covering used in FSM minimization or unate covering used in decomposition to efficient hardware algorithms. This can be done by checking satisfiability [35, 45].

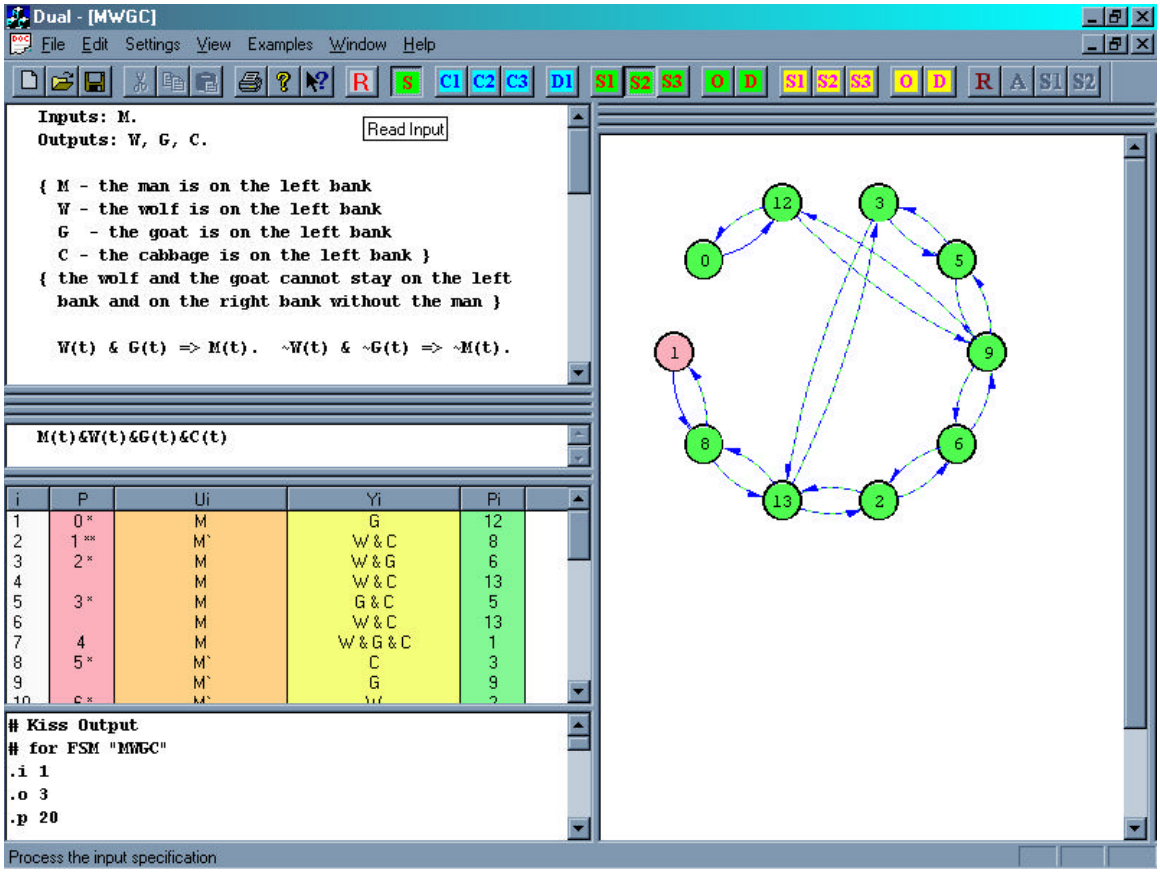
7 Demonstration of learning hardware in robotics, or “improved Furby"

Similar to DeGaris and his ROBOKONEKO robot-kitten, we need a real-life environment to demonstrate the practicality of our ideas. We have chosen the humanoid arms/head robot: a software/hardware machine connected to an inexpensive robot (OWI kits) and a solid-state camera.

Mechanically, the robot will be built from two OWI robotic arms as two hands, and a modified OWI arm as a head. More motors and gears from Robix and LEGO Mindstorms kits will be used for eyes, brows, and ear movements. Thus an upper body of a human puppet will be assembled, controlled by a total of 3 * 5 + 4 * 2 = 23 motors. There will also be several sensors on each hand and the face: temperature, touch, infrared, and others. The

[1] LCA stands for Logic Cell Arrays

Figure 1. DUAL interface for RSM specification and synthesis ("man, wolf, goat, and cabbage" problem)



signals from them will be converted in A/D converters to multi-valued input signals of the reactive state machines.

The robot will perform simple programmable movements such as: MOTOR-1-UP, MOTOR-2-DOWN, MOTOR-3-LEFT, PICK, RELEASE. They correspond to states of output variables. For each OVI arm there are 5 motors, each in 3 states (left, right, none). All signals are programmed as multi-valued. Timing information is added.

At first, we follow the standard "learning from supervisor" approach, with the human as supervisor. He creates all sequences and constraints for the reactive state machine. It is as if the parent teaches the child by directly re-wiring his brain using positive and negative examples. Thus, learning is done with the human as the feedback loop. The set of sequences is incomplete, so the machine performs the *generalization* automatically. Adding or removing new rules, by the human supervisor or automatically/randomly, will change the behavior. What obstacles can the robot's arm encounter? How to react to them? How should the robot react to or mimick the human's behaviors seen by the camera? A lengthy process of trial and error is necessary to answer these questions. The goal of this project is to design a system that reacts to sound, temperature, touch, words (text) from speech recognition [51], simplified images [39], changes of light, etc.

Our interest is to design a system similar to the Furby toy, but capable of real learning. Let us first discuss how Furby works. It can be observed that Furby's internal states are prespecified, its learning is only transiting to prespecified new states in the labyrinth of its possible "states of emotions and knowledge" (sleeps, plays games, sings, is ill/healthy, etc). Appropriate learning patterns (such as petting the head twice and then the back once) lead to displays of appropriate behaviors pre-stored in the toy's memory, and are only hidden from the user by not entering some internal states earlier.

Table 2. Brain Builder versus Universal Logic Machine

Aspect of comparison	Approach to learning hardware	
	Brain Builder	**Universal Logic Machine**
Model of learning	Artificial neural net (ANN)	Reactive state machines (RSMs)
Training data	Sample vectors	Multi-valued temporal logic constraint language L
How the net is constructed	Genetic algorithm, AAN training	RSM construction and minimization, MV logic synthesis
Intermediate representation	Cellular automata (CA)	Regular automata (RA)
What is learned	CA tables	Binary sequential logic nets
Implementation	Hardware (intrinsic EHW)	Hardware and software
Mapped to	Array of binary FPGAs	Array of binary FPGAs
Hardware platform	Xilinx 6000 series CBM	Xilinx 3090, on-board memory, DEC-PERLE-1 board, DEC workstation

Although this is not real learning, it is perceived as astounding by people who observe this toy. Now, we want to create a toy similar in sensor/actuator Pavlovian/Skinnerian learning model, but capable of building its own "world model" and internal model with unlimited behaviors. The new states corresponding to changed behavior will be created using our RSM approach.

The demonstration illustrates an approach to programming robots based on learning from examples. Robot control units (i.e. RSMs) are constructed as a hierarchy of behavior modules concurrently running in a multi-tasking environment. As a result, the robot will exhibit simple actions to which more sophisticated behavior patterns can be added by adding higher-level control. This way of organizing a hierarchy of control modules is known as subsumption architecture. This is a concrete way of introducing multi-tasking and concepts of real-time control to electrical engineering students as it is done at MIT, CMU etc. What is new about our approach, is that the RSM is synthesized (evolved) automatically from input/output relationships specified in our concurrent constraint language.

8 Conclusion

Within the Learning Hardware general philosphy, we have been pursuing the approach called the Universal Logic Machine (ULM). Table 2 shows a comparison between Brain Builder CAM-Brain Machine (CBM) and ULM approaches. We presented an overview of our past and current research as well as the goals of the entire ULM project. Our presentation includes a demonstration of the RSM software.

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